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APPLICATION NO.	FILI	ING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
09/832,867 04/12/2001		/12/2001	Shunpei Yamazaki	740756-2294 1394			
22204	7590	04/21/2003					
NIXON PEA			EXAMINER				
8180 GREEN: SUITE 800	SBOKO D	RIVE		LEWIS, MONICA			
MCLEAN, VA 22102				<del></del>			
•				ART UNIT	PAPER NUMBER		
·				2822			
				DATE MAILED: 04/21/2003	DATE MAILED: 04/21/2003		

Please find below and/or attached an Office communication concerning this application or proceeding.

		<u>**</u>	/				
	,	Application No.	Applicant(s)				
Office Action Summan		09/832,867	YAMAZAKI ET AL.				
Office Action Summary		Examiner	Art Unit				
The MAILING DATE of this comm	I	Monica Lewis	2822				
The MAILING DATE of this communication app ars on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).  Status							
1) Responsive to communication(s	) filed on <i>31 Jar</i>	nuary 2003 .					
2a)⊠ This action is FINAL.		2b)☐ This action is non-final.					
	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. <b>Disposition of Claims</b>							
4)⊠ Claim(s) 1-14 and 25-50 is/are pending in the application.							
4a) Of the above claim(s) is/are withdrawn from consideration.							
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1-14 and 25-50</u> is/are re	jected.						
7) Claim(s) is/are objected to			-				
8) Claim(s) are subject to res	triction and/or e	election requirement.					
Application Papers	<u> </u>						
9) The specification is objected to by the Examiner.							
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
11)⊠ The proposed drawing correction filed on <u>31 January 2003</u> is: a)⊠ approved b)□ disapproved by the Examiner.  If approved, corrected drawings are required in reply to this Office action.							
12) The oath or declaration is objected to by the Examiner.							
Priority under 35 U.S.C. §§ 119 and 120							
13)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).							
a)⊠ All b)□ Some * c)□ None of:							
1.⊠ Certified copies of the priority documents have been received.							
2. Certified copies of the priority documents have been received in Application No							
<ul> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>							
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).							
<ul> <li>a)          The translation of the foreign language provisional application has been received.     </li> <li>15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.</li> </ul>							
Attachment(s)							
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 12.  4) Interview Summary (PTO-413) Paper No(s) 5) Notice of Informal Patent Application (PTO-152) 6) Other:							

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### **DETAILED ACTION**

1. This action is in response to the amendment filed January 31, 2003.

## Response to Arguments

2. Applicant's arguments with respect to claims 1-14 and 25-50 have been considered but are moot in view of the new ground(s) of rejection.

## Claim Objections

3. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

### Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### **Double Patenting**

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686

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F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-14 and 25-50 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim1-13 of copending Application No. 09/837,324. Although the conflicting claims are not identical, they are not patentably distinct from each other because they both deal with light emitting devices.

This is a <u>provisional</u> obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

In regards to claims 1-14, Yamazaki et al. ("Yamazaki") discloses the following:

- a) a channel forming region, n-type forming regions, gate, conductive films of various types and insulating films of various types (See Claims 1-13).

  In regards to claims 25-50, Yamazaki discloses the following:
- a) a channel forming region, n-type forming regions, gate, conductive films of various types, insulating films of various types, coloring layers, light emitting elements, pixels, impurity concentrations (See Claims 1-13).

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# Claim Rejections - 35 USC § 103

- 7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 8. Claims 1, 2, 5-8, 13, 14, 39, 40, 43, 44, 49 and 50 are rejected under 35 U.S.C. 103(a) as obvious over Kamiura et al. (U.S. Patent No. 6,288,413) in view of Toshiba (Japanese Application No. 7-72675).

In regards to claim 1, Kamiura et al. ("Kamiura") discloses the following:

- a) a channel forming region (For Example: See Figure 1F);
- b) an n-type impurity region (5) adjacent to the channel forming region (For Example: See Figure 1F);
- c) an n-type impurity region (11) adjacent to the n-type impurity region (For Example: See Figure 1F);
- d) an n-type impurity region (12) adjacent to the n-type impurity region (For Example: See Figure 1F);
- e) a gate insulating layer (3) provided over the active layer (For Example: See Figure 1F);
- f) a gate electrode (4) provided over the gate insulating layer (For Example: See Figure 1F);
- g) a first conductive film (8) provided over the gate insulating layer (For Example: See Figure 1F); and
- h) first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween (For Example: See Figure 1F).

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In regards to claim 1, Kamiura fails to disclose the following:

a) a second conductive film.

However, Toshiba discloses the use of a second conductive film (See Paragraph 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a second conductive film as disclosed in Toshiba because it aids in improving the element speed (See Paragraph 12).

Additionally, since Kamiura and Toshiba are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Kamiura.

In regards to claim 2, Kamiura discloses the following:

- a) a channel forming region (For Example: See Figure 1F);
- b) an n-type impurity region adjacent to the channel forming region (For Example: See Figure 1F);
- c) an n-type impurity region adjacent to the n-type impurity region (See Figure 1F);
- d) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1F)
- e) a gate insulating layer provided over the active layer (For Example: See Figure 1F);
- f) a gate electrode provided over the gate insulating layer (For Example: See Figure 1F);
- g) a first conductive film provided over the gate insulating layer (For Example: See Figure 1F); and
- h) first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween (For Example: See Figure 1F).

In regards to claim 2, Kamiura fails to disclose the following:

a) a second conductive film.

However, Toshiba discloses the use of a second conductive film (See Paragraph 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a second conductive film as disclosed in Toshiba because it aids in improving the element speed (See Paragraph 12).

Additionally, since Kamiura and Toshiba are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Kamiura.

b) a drive circuit.

However, Toshiba discloses the use of a drive circuit (See Paragraph 25). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a drive circuit as disclosed in Toshiba because it aids in providing high current drive capacity (See Paragraph 25).

Additionally, since Kamiura and Toshiba are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Kamiura.

In regards to claims 5 and 6, Kamiura fails to disclose the following:

a) the first conductive film comprises tungsten, and the second gate electrode comprises aluminum.

However, Toshiba discloses the use of a conductive film comprising tungsten and aluminum (See Paragraph 27). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include conductive film comprising tungsten and aluminum as disclosed in Toshiba because it aids in providing a low contact resistance (See Paragraph 12).

Additionally, since Kamiura and Toshiba are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Kamiura.

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In regards to claims 7 and 8, Kamiura fails to disclose the following:

a) the n-type impurity region includes an n-type impurity element in concentrations from  $1\times10^{20}$  to  $1\times10^{21}$  atoms/cm<sup>3</sup>, the n-type doped region includes an n-type impurity element in concentrations of from  $2\times10^{16}$  to  $5\times10^{19}$  atoms/cm<sup>3</sup>, and the n-type doped region includes an n-type impurity element in concentrations from  $1\times10^{16}$  to  $5\times10^{19}$  atoms/cm.<sup>3</sup>

However, the applicant has not established the critical nature of concentrations from  $1x10^{20}$  to  $1x10^{21}$  atoms/cm<sup>3</sup>,  $2x10^{16}$  to  $5x10^{19}$ atoms/cm<sup>3</sup>, and  $1x10^{16}$  to  $5x10^{19}$ atoms/cm<sup>3</sup>. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claims 13 and 14, Kamiura discloses the following:

a) the light emitting device is selected from the group consisting of an EL display, a video camera, a digital camera, a portable computer, a personal computer, a portable telephone, and a car audio stereo (See Column 1 Lines 14-19).

In regards to claim 39, Kamiura discloses the following:

- a) a semiconductor island on an insulating surface over the substrate (For Example: See Figure 1F);
- b) source and drain regions formed in the semiconductor island (For Example: See Figure 1F);
- c) a channel region in the semiconductor island between the source and drain regions (For Example: See Figure 1F);
- d) a pair of lightly doped regions formed between the channel region and the source and drain regions (For Example: See Figure 1F);
- e) a gate electrode formed over the semiconductor island with a gate insulating film interposed therebetween (For Example: See Figure 1F);

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f) a first conductive film (For Example: See Figure 1F); and

g) the channel region is overlapped by the first conductive film wherein the portions of each of the pair of lightly doped regions are overlapped by the first conductive film, are not overlapped by the gate electrode (For Example: See Figure 1F).

In regards to claim 39, Kamiura fails to disclose the following:

a) a second conductive film.

However, Toshiba discloses the use of a second conductive film (See Paragraph 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a second conductive film as disclosed in Toshiba because it aids in improving the element speed (See Paragraph 12).

Additionally, since Kamiura and Toshiba are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Kamiura.

In regards to claim 40, Kamiura discloses the following:

- a) a semiconductor island on an insulating surface over the substrate (For Example: See Figure 1F);
- b) source and drain regions formed in the semiconductor island (For Example: See Figure 1F);
- c) a channel region in the semiconductor island between the source and drain regions (For Example: See Figure 1F);
- d) a pair of lightly doped regions formed between the channel region and the source and drain regions (For Example: See Figure 1F);
- e) a gate electrode formed over the semiconductor island with a gate insulating film interposed therebetween (For Example: See Figure 1F);
  - f) a first conductive film (For Example: See Figure 1F); and
- g) the channel region is overlapped by the first conductive film wherein the portions of each of the pair of lightly doped regions are overlapped by the first conductive film, are not overlapped by the gate electrode (For Example: See Figure 1F).

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In regards to claim 40, Kamiura fails to disclose the following:

a) a second conductive film.

However, Toshiba discloses the use of a second conductive film (See Paragraph 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a second conductive film as disclosed in Toshiba because it aids in improving the element speed (See Paragraph 12).

Additionally, since Kamiura and Toshiba are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Kamiura.

b) a drive circuit.

However, Toshiba discloses the use of a drive circuit (See Paragraph 25). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a drive circuit as disclosed in Toshiba because it aids in providing a thin film transistor with high current drive capacity (See Paragraph 25).

Additionally, since Kamiura and Toshiba are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Kamiura.

In regards to claims 43 and 44, Takemura fails to disclose the following:

a) the first conductive film comprises tungsten, and the second gate electrode comprises aluminum.

However, Toshiba discloses the use of a conductive film comprising tungsten and aluminum (See Paragraph 27). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Huang to include conductive film comprising tungsten and aluminum as disclosed in Toshiba because it aids in providing a low contact resistance (See Paragraph 12).

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Additionally, since Kamiura and Toshiba are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Kamiura.

In regards to claims 49 and 50, Kamiura discloses the following:

- a) the light emitting device is selected from the group consisting of an EL display, a video camera, a digital camera, a portable computer, a personal computer, a portable telephone, and a car audio stereo (See Column 1 Lines 14-19).
- 9. Claims 3, 4, 41 and 42 are rejected under 35 U.S.C. 103(a) as obvious over Kamiura et al. (U.S. Patent No. 6,288,413) in view of Toshiba (Japanese Application No. 7-72675) and Yamazaki et al. (U.S. Patent No. 5,627,084).

In regards to claims 3 and 4, Kamiura fails to disclose the following:

a) the first conductive film comprises one of tantalum nitride and titanium nitride, and the second gate electrode comprises tungsten.

However, Yamazaki et al. ("Yamazaki") discloses the use of various conductive films comprising tantalum, titanium, and tungsten (See Column 3 Lines 7-43 and Column 5 Lines 14-24). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include various conductive films comprising tantalum, titanium, and tungsten as disclosed in Yamazaki because it aids in forming the gate electrode (See Column 3 Lines 7-43 and Column 5 Lines 14-24).

Additionally, since Kamiura and Yamazaki are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Yamazaki.

In regards to claims 41 and 42, Kamiura fails to disclose the following:

a) the first conductive film comprises one of tantalum nitride and titanium nitride, and the second gate electrode comprises tungsten.

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However, Yamazaki discloses the use of various conductive films comprising tantalum, titanium, and tungsten (See Column 3 Lines 7-43 and Column 5

Lines 14-24). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include various conductive films comprising tantalum, titanium, and tungsten as disclosed in Yamazaki because it aids in forming the gate electrode (See Column 3 Lines 7-43 and Column 5

Lines 14-24).

Additionally, since Kamiura and Yamazaki are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Yamazaki.

10. Claims 9, 10, 45 and 46 are rejected under 35 U.S.C. 103(a) as obvious over Kamiura et al. (U.S. Patent No. 6,288,413) in view of Toshiba (Japanese Application No. 7-72675) and Zhang (U.S. Patent No. 5,717,224).

In regards to claims 9 and 10, Kamiura fails to disclose the following:

a) the gate electrode is covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride films.

However, Zhang discloses a gate electrode covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride film (See Column 8 Lines 44-47). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a gate electrode covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride film as disclosed in Zhang because it aids in keeping the device from shortening out (For Example: See Figure 3c).

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Additionally, since Kamiura and Zhang are both from the same field of endeavor, the purpose disclosed by Zhang would have been recognized in the pertinent art of Kamiura.

In regards to claims 45 and 46, Kamiura fails to disclose the following:

a) the gate electrode is covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride films.

However, Zhang discloses a gate electrode covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride film (See Column 8 Lines 44-47). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a gate electrode covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride film as disclosed in Zhang because it aids in keeping the device from shortening out (For Example: See Figure 3c).

Additionally, since Kamiura and Zhang are both from the same field of endeavor, the purpose disclosed by Zhang would have been recognized in the pertinent art of Kamiura.

11. Claims 11, 12, 47 and 48 are rejected under 35 U.S.C. 103(a) as obvious over Kamiura et al. (U.S. Patent No. 6,288,413) in view of Toshiba (Japanese Application No. 7-72675), Zhang (U.S. Patent No. 5,717,224) and Shohara et al. (U.S. Patent No. 6,238,754).

In regards to claims 11 and 12, Kamiura fails to disclose the following:

a) a coloring layer is provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitride film.

However, Shohara discloses a coloring layer provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitride film (See Column 13

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Lines 7-35). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a coloring layer provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitiride film as disclosed in Shohara because it aids in providing good display characteristics (See Column 13 Lines 7-35).

Additionally, since Kamiura and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Kamiura.

In regards to claims 47 and 48, Kamiura fails to disclose the following:

a) a coloring layer is provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitiride film.

However, Shohara discloses a coloring layer is provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitiride film (See Column 13 Lines 7-35). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a coloring layer is provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitiride film as disclosed in Shohara because it aids in providing good display characteristics (See Column 13 Lines 7-35).

Additionally, since Kamiura and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Kamiura.

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12. Claims 25, 26, 29-32 and 35-38 are rejected under 35 U.S.C. 103(a) as obvious over Kamiura et al. (U.S. Patent No. 6,288,413) in view of Toshiba (Japanese Application No. 7-72675) and Shohara et al. (U.S. Patent No. 6,238,754).

In regards to claim 25, Kamiura discloses the following:

- a) a channel forming region (For Example: See Figure 1F);
- b) an n-type impurity region adjacent to the channel forming region (For Example: See Figure 1F);
- c) an n-type impurity region adjacent to the n-type impurity region (See Figure 1F);
- d) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1F)
- e) a gate insulating layer provided over the active layer (For Example: See Figure 1F);
- f) a gate electrode provided over the gate insulating layer (For Example: See Figure 1F);
- g) a first conductive film provided over the gate insulating layer (For Example: See Figure 1F); and
- h) first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween (For Example: See Figure 1F).

In regards to claim 25, Kamiura fails to disclose the following:

a) a second conductive film.

However, Toshiba discloses the use of a second conductive film (See Paragraph 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a second conductive film as disclosed in Toshiba because it aids in improving the element speed (See Paragraph 12).

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Additionally, since Kamiura and Toshiba are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Kamiura.

b) a coloring layer

However, Shohara discloses a coloring layer (See Column 13 Lines 7-35). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a coloring layer as disclosed in Shohara because it aids in providing good display characteristics (See Column 13 Lines 7-35).

Additionally, since Kamiura and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Kamiura.

In regards to claim 26, Kamiura discloses the following:

- a) a channel forming region (For Example: See Figure 1F);
- b) an n-type impurity region adjacent to the channel forming region (For Example: See Figure 1F);
- c) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1F);
- d) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1F)
- e) a gate insulating layer provided over the active layer (For Example: See Figure 1F);
- f) a gate electrode provided over the gate insulating layer (For Example: See Figure 1F);
- g) a first conductive film provided over the gate insulating layer (For Example: See Figure 1F); and
- h) first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween (For Example: See Figure 1F).

In regards to claim 26, Kamiura fails to disclose the following:

a) a second conductive film.

However, Toshiba discloses the use of a second conductive film (See Paragraph 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a second conductive film as disclosed in Toshiba because it aids in improving the element speed (See Paragraph 12).

Additionally, since Kamiura and Toshiba are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Kamiura.

b) a drive circuit.

However, Toshiba discloses the use of a drive circuit (See Paragraph 25). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a drive circuit as disclosed in Toshiba because it aids in providing high current drive capacity (See Paragraph 25).

Additionally, since Kamiura and Toshiba are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Kamiura.

c) a coloring layer

However, Shohara discloses a coloring layer (See Column 13 Lines 7-35). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a coloring layer as disclosed in Shohara because it aids in providing good display characteristics (See Column 13 Lines 7-35).

Additionally, since Kamiura and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Kamiura.

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In regards to claims 29 and 30, Kamiura fails to disclose the following:

a) the first conductive film comprises tungsten, and the second gate electrode comprises aluminum.

However, Toshiba discloses the use of a conductive film comprising tungsten and aluminum (See Paragraph 27). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include conductive film comprising tungsten and aluminum as disclosed in Toshiba because it aids in providing a low contact resistance (See Paragraph 12).

Additionally, since Kamiura and Toshiba are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Kamiura.

In regards to claims 31 and 32, Kamiura fails to disclose the following:

a) the n-type impurity region includes an n-type impurity element in concentrations from  $1 \times 10^{20}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>, the n-type doped region includes an n-type impurity element in concentrations of from  $2 \times 10^{16}$  to  $5 \times 10^{19}$  atoms/cm<sup>3</sup>, and the n-type doped region includes an n-type impurity element in concentrations from  $1 \times 10^{16}$  to  $5 \times 10^{19}$  atoms/cm.<sup>3</sup>

However, the applicant has not established the critical nature of concentrations from  $1 \times 10^{20}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>,  $2 \times 10^{16}$  to  $5 \times 10^{19}$  atoms/cm<sup>3</sup>, and  $1 \times 10^{16}$  to  $5 \times 10^{19}$  atoms/cm<sup>3</sup>. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claims 35 and 36, Kamiura fails to disclose the following:

a) a coloring layer is provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitiride film.

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However, Shohara discloses a coloring layer provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitiride film (See Column 13 Lines 7-35). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a coloring layer provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitiride film as disclosed in Shohara because it aids in providing good display characteristics (See Column 13 Lines 7-35).

Additionally, since Kamiura and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Kamiura.

In regards to claims 37 and 38, Kamiura discloses the following:

- a) the light emitting device is selected from the group consisting of an EL display, a video camera, a digital camera, a portable computer, a personal computer, a portable telephone, and a car audio stereo (See Column 1 Lines 14-19).
- 13. Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as obvious over Kamiura et al. (U.S. Patent No. 6,288,413) in view of Toshiba (Japanese Application No. 7-72675), Shohara et al. (U.S. Patent No. 6,238,754) and Yamazaki et al. (U.S. Patent No. 5,627,084).

In regards to claims 27 and 28, Kamiura fails to disclose the following:

a) the first conductive film comprises one of tantalum nitride and titanium nitride, and the second gate electrode comprises tungsten.

However, Yamazaki discloses the use of various conductive films comprising tantalum, titanium, and tungsten (See Column 3 Lines 7-43 and Column 5

Lines 14-24). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include various

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conductive films comprising tantalum, titanium, and tungsten as disclosed in Yamazaki because it aids in forming the gate electrode (See Column 3 Lines 7-43 and Column 5 Lines 14-24).

Additionally, since Kamiura and Yamazaki are both from the same field of endeavor, the purpose disclosed by Toshiba would have been recognized in the pertinent art of Yamazaki.

14. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as obvious over Kamiura et al. (U.S. Patent No. 6,288,413) in view of Toshiba (Japanese Application No. 7-72675), Shohara et al. (U.S. Patent No. 6,238,754) and Zhang (U.S. Patent No. 5,717,224).

In regards to claims 33 and 34, Kamiura fails to disclose the following:

a) the gate electrode is covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride films.

However, Zhang discloses a gate electrode covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride film (See Column 8 Lines 44-47). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kamiura to include a gate electrode covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride film as disclosed in Zhang because it aids in keeping the device from shortening out (For Example: See Figure 3c).

Additionally, since Kamiura and Zhang are both from the same field of endeavor, the purpose disclosed by Zhang would have been recognized in the pertinent art of Kamiura.

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a semiconductor device.

Conclusion

15. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Yamazaki (Japanese Publication No. 2000223716) discloses a semiconductor device; b) Yamazaki et al. (Japanese Publication No. 2000236097) discloses a semiconductor device; and c) Yamazaki et al. (Japanese Publication No. 2000243975) discloses

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML April 16, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

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